REMARKS

By way of the present response, claims 1, 2, 8-10, 12, 17 and 19 are amended. Claims 1-20 currently are pending.

Support for the amendments are provided in at least Figures 1 and 2 and related text of the specification. No new matter has been added. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

The Office Action includes an objection to the drawings for not showing a low noise resistivity circuit including an analog circuit. While Applicants submit that the depiction of a particular analog circuit would not be necessary for one of ordinary skill in the art to understand the invention, the claims have been broadened such that they do not explicitly recite a low noise resistivity circuit including an analog circuit. It is respectfully submitted that the present amendments render moot the objection to the drawings.

Claims 1-20 are rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Ohie (U.S. Patent No. 6,580,164) in view of Gutierrez (U.S. Patent No. 6,879,023). To the extent the Office may consider this rejection to apply to the amended claims, Applicants respectfully traverse.

Starting with amended independent claims, claim 1 recites, among other things, the feature of a second circuit area that includes a circuit subject to noise and is positioned between the first electrode group and the second electrode group. Additionally, amended claim 1 recites that the first electrode group is electrically connected to the third electrode group of the second semiconductor chip and that the second electrode group is electrically connected to the external connection terminals. It is respectfully submitted that the Ohie patent does not describe, imply or suggest that a circuit is included in an area or a region between the pad electrodes 125 and the first pad electrodes 105. Moreover, the Gutierrez patent fails to cure the deficiencies of Ohie.

Gutierrez teaches that a digital circuit area (i.e., items 214 or 314) and an analog circuit area (i.e., items 216 or 316) are arranged to prevent transmission of noise directly to one another by way of a substrate barrier or substrate island in the substrate between the respective circuit areas. That is, Gutierrez teaches that the analog circuit area (216 or 316) is positioned in relation to the digital circuit area (214 or 314) at some interval defined by the substrate barrier or the substrate island. However, the Gutierrez patent does not mention or suggest how the analog circuit area (216 or 316) is positioned in relation to electrodes of the

semiconductor die 310. Hence, Gutierrez does not teach or suggest how the analog circuit area (216 or 316) is positioned in relation to both the electrodes that are electrically connected to external connection terminals of the semiconductor die 310, and the electrodes that are electrically connected to a semiconductor die different from the semiconductor die 310. Consequently, even if one were to consider, for the sake of argument, combining the Ohie and Gutierrez patents, such a hypothetical combination would not have led of ordinary skill in the art to position the analog circuit area as described in Gutierrez between the pad electrodes (i.e., item 125) and the first pad electrodes (item 105) of the Ohie patent.

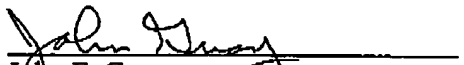
Similar distinctions are recited in each of independent claims 2 and 10. For example, claim 2 recites the feature of a second circuit element region that includes a circuit subject to noise and is positioned between the first electrodes and the second electrodes. In addition, claim 2 recites that the first electrodes are electrically connected to the third electrodes of the second semiconductor chip, and that the second electrodes are electrically connected to the external connection terminals. Claim 10 recites the feature of a second circuit area that includes a circuit subject to noise and is positioned between the first electrodes and the second electrodes. Claim 10 also recites that the first electrodes are electrically connected to the third electrodes of the second semiconductor chip, and that the second electrodes are electrically connected to the external connection terminals. Therefore, claims 2 and 10 are believed allowable reasons analogous to those given above with respect to claim 1.

Accordingly, Applicants respectfully submit that the rejection of all independent claims is rendered moot and obviated in view of the amendments.

The remaining claims depend from one of independent claims 1, 2 and 10, and are therefore considered allowable at least for the above reasons, and further for the additional features recited.

The present application is now believed to be in condition for allowance, and prompt notification of the same is earnestly sought.

Respectfully submitted,



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